In System Programming Evaluation Kit Specification

V1.1

IMPORTANT:

Reader must first refer to our Application Note: AN0103 “On-board SPI programming with DediProg tools: Designer version” to have a full understanding on the In System Programming methods and implementation in the application.

The present specification aims to explain how to evaluate the In System Programming method with your current application board and controller without any hardware change required.

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I. Introduction

The Serial Flash memories are the optimized solution for applications using code shadowing in RAM or “none critical performance code” for Xip due to their low cost, low pin count and small application impact.
Update flexibility is often required for convenient development, debugging and production.
We can clearly differentiate 3 different solutions on the market:

1) **Socket:**
   The socket is soldered in place of the serial Flash so that when the update is needed, the memories can be removed and updated in an Engineering programmer like our SF200 programmer.

   Advantages:
   - Applicable to all the applications

   Disadvantages:
   - Not applicable in volume (high cost)
   - Not convenient (part to be removed, updated and inserted again)
   - Problem of signals integrity (Contact, oxidation…)

2) **In system Programming via the application controller.**
   Some chipsets or controllers provide a way to update the Serial Flash on board.
   This is usually performed by connecting a dedicated tool provided by the chipset suppliers to a slow bus in the application (JTAG, UART...) to control the Serial Flash update through the chipset.

   Advantages:
   - Supported by the controller supplier

   Disadvantages:
   - Slow performances:
     ➔ Communication between tool and controller with slow bus (often I2C)
     ➔ Followed by the communication between controller and Serial Flash with a slow programming (program by small packets of data).
   - Usually not applicable in volume (high cost due to connector and slow programming time)
   - Require an extra bus on the application for this purpose

3) **Direct In system Programming via the SPI bus**
   DediProg programmer is connected directly on the SPI bus of the Serial Flash and ensures an update with the highest flexibility and performances.

   Advantages:
   - High Performance (SPI tool optimised for serial Flash)
   - Convenient for development and debugging (no extra manipulation)

Requirement:

- Solution needs to be validated with the application hardware and controller by using our ISP evaluation board

II. DediProg ISP solutions

You and your customers will benefit of the highest update flexibility for development, debugging, production and repairing by using our In system Programming method allowing to reduce the time to market.

Features: update your SPI Flash soldered on your application board by using our dedicated programmers: **SF100** and **SF100+.** When connected to the application board, the **SF100** programmer can control the SPI bus to read or update the Serial Flash content.

1) The programmer can be connected on the application ISP connector:

Fig 1: In System Programming update with connector on board

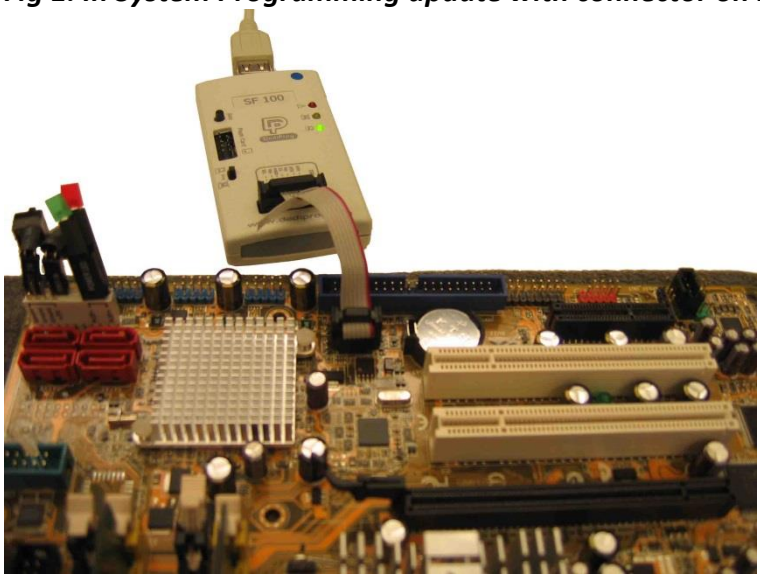


Fig 2: ISP connector example (2.54mm or 1.27mm pitch)

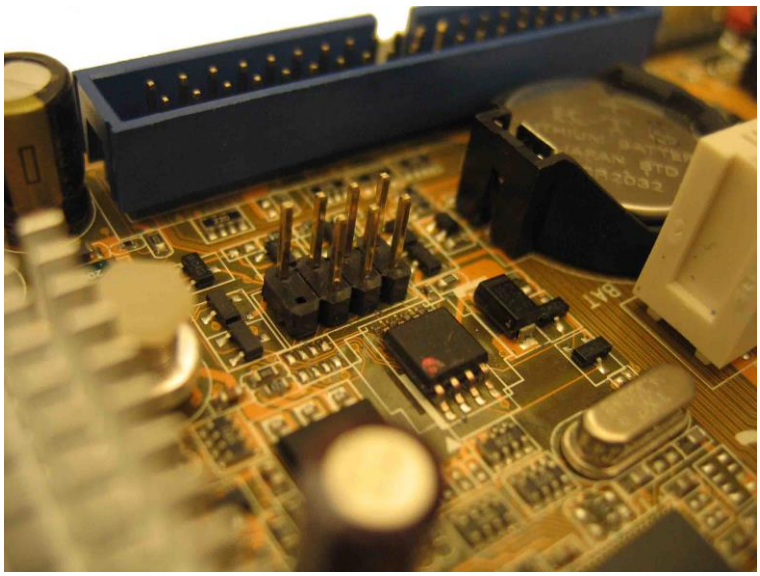
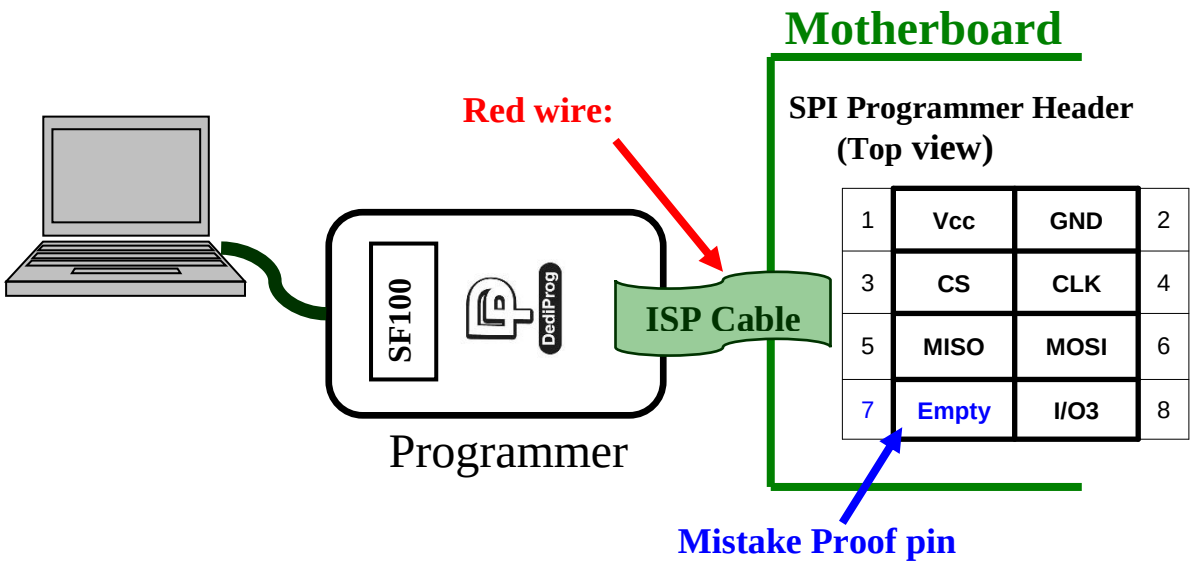


Fig 3: Standard Connector pin out



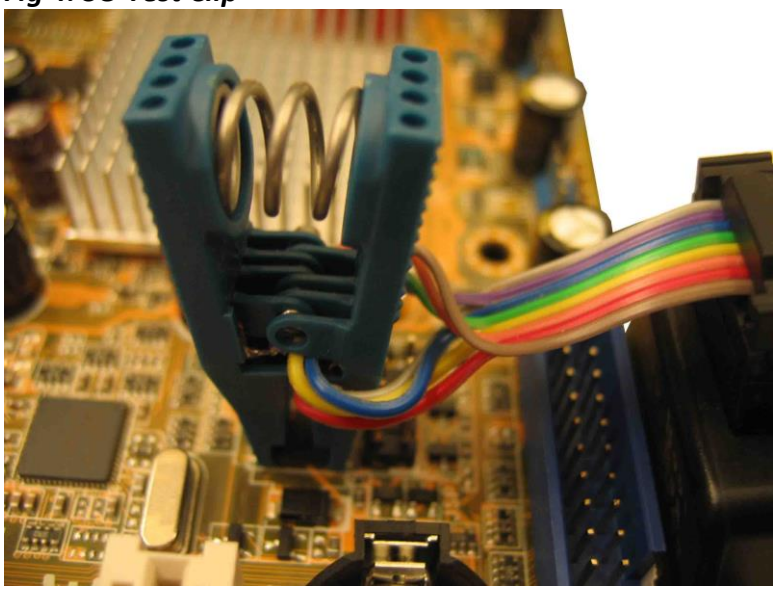
Tab 1: Description of the signals:

Pin	Name of signal	Description
1, 2	Vcc, Gnd	Vcc supplied from the programmer to the Serial Flash
3, 4, 5, 6	CS1, CLK, MISO, MOSI	SPI signals
5	Vcc	Vcc is used to supply the application memory
8	IO3	Used to reset the Chipset or switch off the Mosfet
7	Mistake proof pin	Prevent from wrong connection

2) The Programmer can also been connected directly on the Serial Flash package

The connection can also be ensured by using our SO test Clip directly connected on the Serial Flash SO8N, SO8W or SO16 packages (no application connector needed).
The SO Test Clip solution can be used for the Mass production in order to save the Pin header. For development purpose, the ISP connector will ensure a better contact stability.

Fig 4: SO Test Clip



III. Why evaluating the ISP with your application?

The direct ISP method will require a minimum of validation. Actually, the SF100 programmer is taking control of the SPI bus and Memory power supply so it is mandatory to check if there is no possible conflict with the application controller (SPI master) or with the application Hardware.

Our ISP Evaluation tool has been designed to test and validate the In System Programming method on your current application board without any hardware change required.

You are:

1) Silicon supplier (Controller, chipset, ASIC, FPGA)

You can easily use our ISP Evaluation tool to check if your current controller, Chipset or Asic is tolerant to the ISP method. You can also ensure that your next chip generation will be compatible with the ISP method.

When supported, this ISP feature will offer a significant advantage to your products for the benefits of your customers: development, production, update, repairing..

Due to its high update flexibility and performance, it will ensure them the shortest time to market.

Do not hesitate to contact our Support team for further explanation.
As soon as your chipset has been validated with our ISP evaluation tool, please forward us the references to be added on our validation list. This will be helpful for your customer references.

2) Application supplier (R&D, designer, Software engineers..)

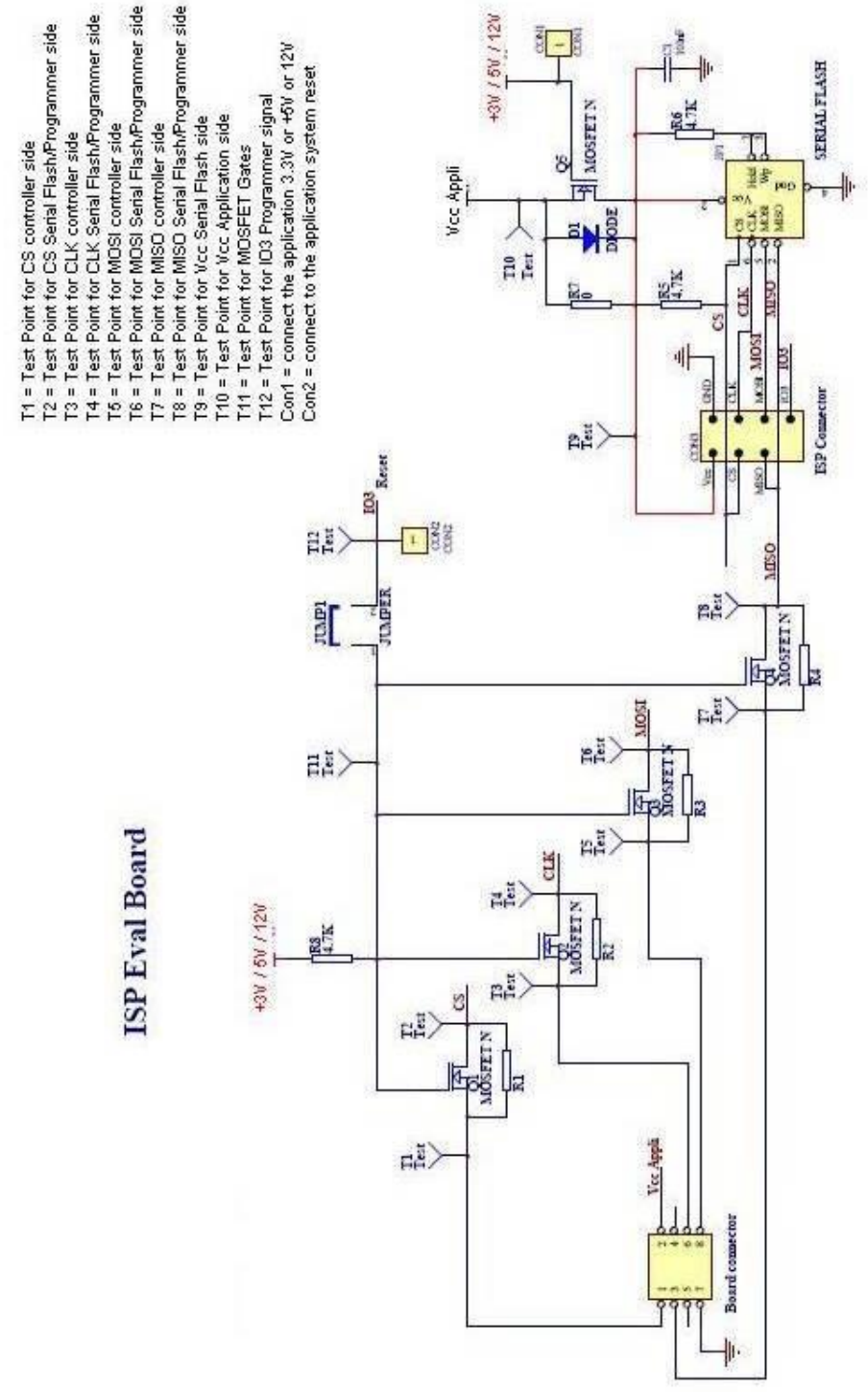
You can follow the instruction below to check if the controller you are using and if your application hardware is compatible with the ISP method. Your company and your customers will benefit of this high flexibility of code update.

You can contact your silicon suppliers to check if they have validated the direct ISP updating method on their chip and in which conditions (see below for explanation). Do not hesitate to forward them the present specification.
You can also contact us (**support@dediprog.com**) to know if your controller supplier is already on our validated list.

IV. ISP Evaluation tool description:

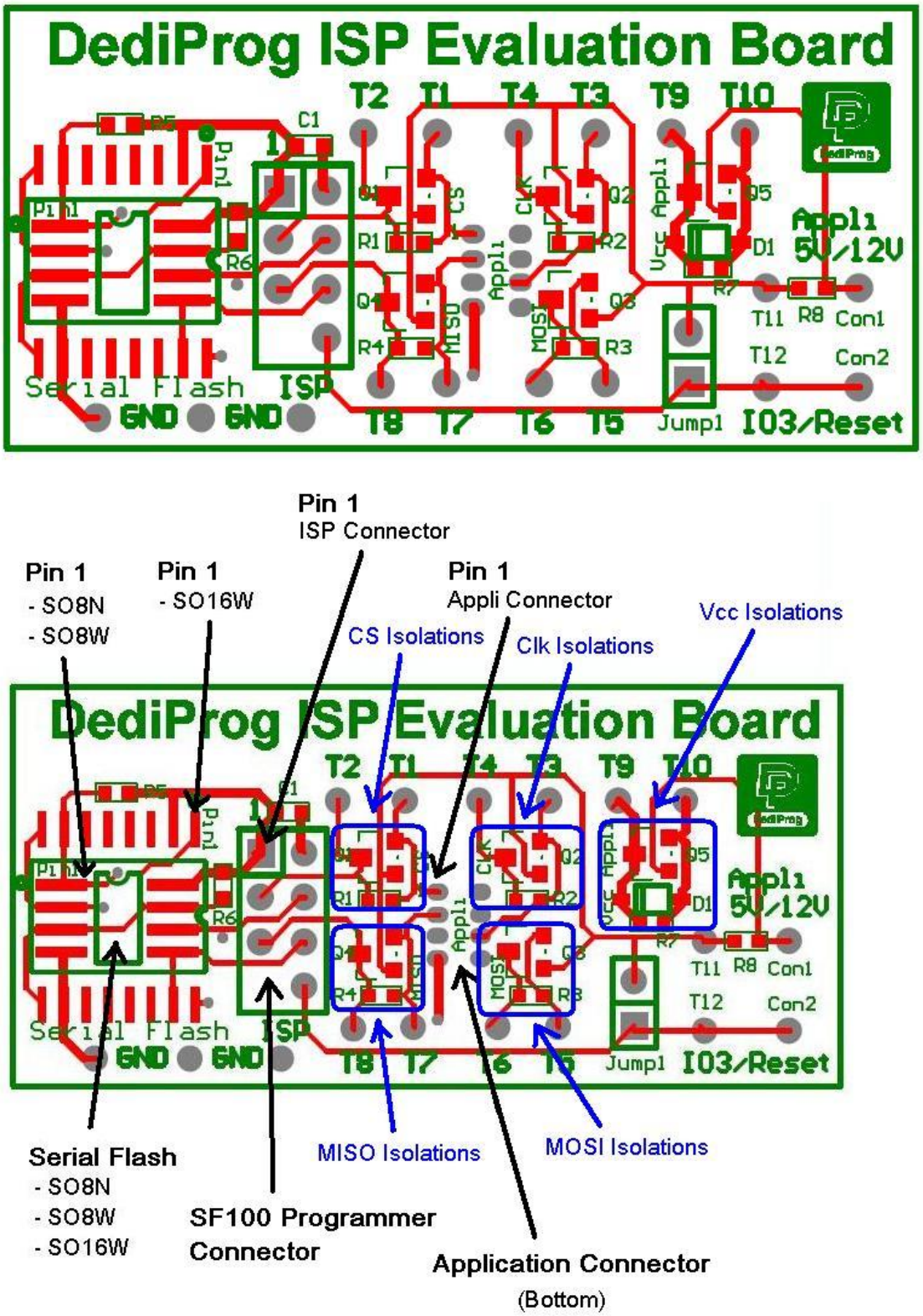
The ISP Evaluation board has been designed to test the Serial Flash ISP update and check the signals quality in any application using the Serial Flash without any hardware change required

Fig 5: Evaluation board schematic



When delivered only R5 (pull-up on CS), R6 (pull-up on Hold and Wp), R8 (pull-up on Mosfet gate) and C1 (serial Flash decoupling) are connected. Others components will have to be soldered by the user according to the test on going.

Fig 6: Evaluation board Top Layout



4.1 SPI isolations

The Serial Flash is soldered on the ISP evaluation board and its SPI signals are directly connected to the ISP connector where the SF100 programmer will be plugged.

The Serial Flash SPI signals are connected to the Application Connector through Serial resistors or Mosfets:
- Chip Select through R1 (serial resistor) or Q1 (Mosfet)
- Clock through R2 (serial resistor) or Q2 (Mosfet)
- MOSI (Master Out Slave In) through R3 (serial resistor) or Q3 (Mosfet)
- MISO (Master In Slave Out) through R4 (serial resistor) or Q4 (Mosfet)

These resistors or Mosfet will ensure the isolation between the controller and the programmer in different scenarios.

MOSFET on SPI

You can solder the Mosfet (Q1, Q2, Q3 and Q4) if you want to evaluate the ISP with Chipset isolated by Mosfet.
For example:
- When the application is OFF, the MOSFET are turn OFF (Gate not supplied) and ensure a perfect isolation between the programmer and the chipset to avoid any leakage in the chipset during the Serial Flash update.
- When the application is ON, the MOSFET can be turned OFF by driving the Gate low via the programmer IO3 and ensure a perfect isolation between the programmer and the chipset to avoid any conflict on the SPI bus during the Serial Flash update.

This method works with all the applications and all the chipsets.
See AN0103 for more details.

SERIAL Resistors on SPI

You can solder the serial resistors (R1, R2, R3 and R4) on the SPI bus to evaluate the chipset tolerance to the ISP update method. Actually, the Resistors will limit the current between the chipset and the programmer in case of leakage or conflict and will be also used to measure the current injected in the chipset. The resistor value will be selected first with high value (100 Ohm or 200 Ohm) for safe ISP trials and tuned to lower value (33 Ohm or 47 Ohm) to reduce the SPI signals filtering during the application life.

Remark: Serial resistors on the SPI bus are always recommended in the application to filter the overshoot and undershoot of the SPI bus and ensure a clean SPI signal.

4.2 Power supply isolation

Update with application OFF:

The SF100 programmer can supply the memory during the update via the Vcc line.

- If the application Vcc is not connected to the ISP evaluation board on T1, the serial flash can be updated by the programmer (programmer supply) but the application will not be able to boot on the Serial Flash.

- If the application Vcc is connected to the ISP evaluation board on T1, The application (OFF during the update) must been protected from the programmer Vcc (3.3V) by soldering the diode (D1) or the Mosfet (Q5) and not R7:
  - With D1, the Vcc can be supplied from the application to the memory for the boot but not from the programmer to the application during the ISP update. The diode must be selected with a small threshold drop down to ensure a good memory supply (2.7V min) when application is ON.
  - With Q5, the Mosfet gate signal (Con1) must been connected to the application power supply (3.3V or 5V or 12V) so that when the application is ON, the MOSFET will be Turn ON to connect the application Vcc to the memory and when the application is OFF the MOSFET will turn OFF and will prevent the programmer to supply the application.

Update with application ON:

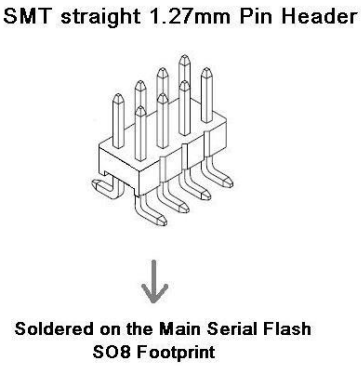
The application can supply the memory during the update operation via the Vcc line. In this case, the resistor R7 (0 Ohm) must be soldered. The programmer Vcc is protected against power conflict during the update.

4.3 Board and application Preparation:

Step 1:
Remove the supply from the application.

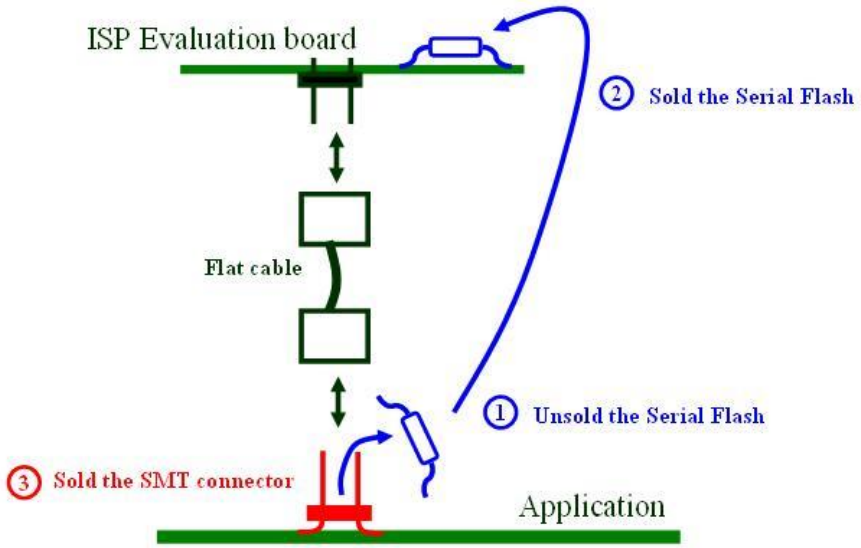
Step 2:
Remove the main serial Flash from the application and solder the DediProg SMT 1.27mm connector compatible with the SO8 footprint.

Fig 7: SMT connector



Step 3:
Solder the Serial Flash on the ISP evaluation board by taking care of the orientation (pin 1 on the dot).

Fig 8: SMT connector soldered on the application Serial Flash footprint



Step 4:
Prepare the ISP evaluation board according to your experiments (see following sections).

Step 5:
When ready, the ISP evaluation board is connected to the SMT application connector via the dedicated cable provided in the kit.

V. How to Use our ISP Evaluation tool?

User can test different ways to update the Serial Flash content with the ISP methods.

Overview:

1. **Update with Power OFF and resistors for SPI isolations**
   Advantages: Low cost and SPI filtering
   Requirements: Need to check the Controller IO tolerance, need Vcc isolation

2. **Update with Power ON and resistors for SPI isolations**
   Advantages: Low cost, SPI filtering and no need of Vcc isolation
   Requirements: Need to check the Controller conditions for high impedance, Application supply is needed

3. **Update with Power OFF and MOSFET for isolations**
   Advantages: Works with all the controllers and applications
   Requirements: 5 Mosfet for SPI and Vcc isolations
4. **Update with Power ON and MOSFET for SPI isolations**
   Advantages: Works with all the controllers and applications
   Requirements: 3 Mosfet for SPI (no need for Vcc and MISO), Application supply is needed

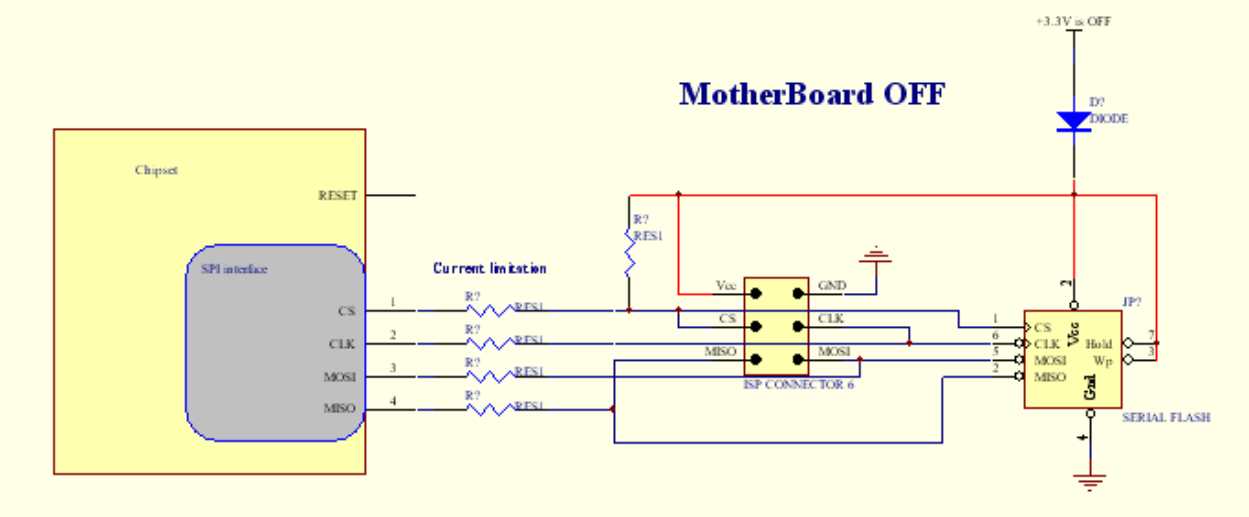
5. **Update with Power OFF or ON and MOSFET for isolations**
   Advantages: Works with all the controllers and applications
   Requirements: 5 Mosfet for SPI and Vcc isolations

Refer to AN0103 for detailed information.

5.1 ISP update with application OFF and resistors isolation

The application board, controller and the Serial Flash are not supplied by the application. In this case, the memory supply will be ensured by the Programmer during the duration of the update. Serial Resistors on SPI bus are used to filter the overshoot and undershoot of the application and isolate the programmer from the controller during the ISP update.

Fig 9: Equivalent schematic for the Application



5.1.1 ISP Update control

Step 1:
Remove the supply from the application.

Step 2:
Solder 100 Ohm serial resistors on the ISP evaluation board SPI bus (R1, R2, R3 and R4) of the ISP evaluation board. 100 Ohm will protect the application controller from leakage current during the update and will be helpful to measure the current injected. Actually, as the application controller is not supplied during the serial flash update, a small current leakage can occur on its SPI Input and output due to the SPI signals level driven by the programmer during the update.

Step 3:
Select the Vcc isolation:
As the programmer will supply the Vcc to the memory during the update, the application (OFF) must be isolated from it.

1) User can solder a Diode D1 on the ISP evaluation board so that the Vcc cannot be supplied from the programmer to the application but can still be supplied from the application to the Serial Flash when the Application is powered. The diode must been selected with a small threshold so that the application Vcc will still be compliant with the serial Flash specification (2.7 to 3.6V).
2) User can solder one N Mosfet Q5 on the ISP evaluation board for the Vcc isolation. The gate of the Mosfet is supplied by the application power (Vcc, 5V or 12V). So that when the application is not supplied, the MOSFET are switch OFF and prevent the programmer Vcc to supply the application board. When the application is supplied then the MOSFET is switched ON and the application Vcc can supply the memory.

One of this two methods must be selected and R7 must been kept empty.

Step 4:
Connect the ISP evaluation board to the application SMT connector by using the dedicated cable provided with the kit.

Step 5:
Connect the application power signals to the ISP evaluation board (keep the application power off):

- Application Vcc (3V or 3.3V) to T10
- Application Vcc or application 5V or 12V to Con1 in case the Mosfet has been selected for the Vcc isolation (Q5). High Voltage will ensure a small Ron so a smaller Vcc drop down.

Step 6:
Connect the SF100 in the ISP connector of the ISP evaluation board.
Take care of the wrong connection (Fig3 and fig6)

Step 7:
Connect the oscilloscope probes to measure the voltage on each SPI Serial resistors:
- On T1 and T2 to measure the threshold on R1 on Chip Select during the programmer communication with the Serial Flash.
- On T3 and T4 to measure the threshold on R2 on Clock during the programmer communication with the Serial Flash.
- On T5 and T6 to measure the threshold on R3 on MOSI during the programmer communication with the Serial Flash.
- On T7 and T8 to measure the threshold on R4 on MISO during the programmer communication with the Serial Flash.

Step 8:
Launch the Serial flash update from the DediProg software and trig the oscilloscope to measure the voltage through the resistors.

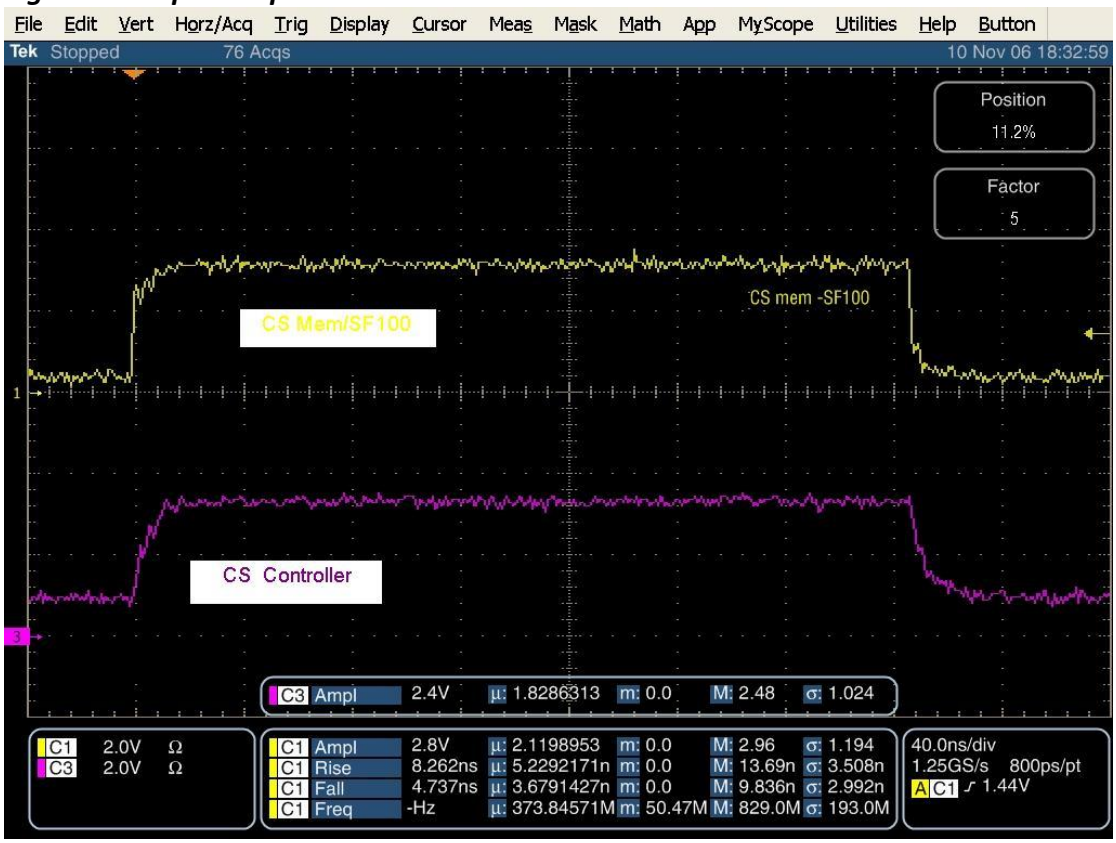
Results Analysis:

- Communication for the Serial Flash update (between Programmer and Serial flash): SPI signals captured on T2, T4, T6 and T8 are used for the update. User must check their integrity taking into account that the ISP evaluation board increase the SPI bus capacitance (Worst case compare to the application).

Remark: T1, T3, T5 and T7 signals (after the resistors) are not used for the update and don't have to be considered (programmer doesn't attempt to communicate with the controller).

- Current measurement:
User has to measure the voltage through each SPI Serial resistors by calculating the difference of voltage between T1 and T2, T3 and T4, T5 and T6 then T7 and T8.
The Voltage through the Serial resistor will indicate the current injected in the controller IO during the short updating Time: I = U/R.

Fig 10: Example: Chip Select



The Yellow signal is the chip select from programmer to the serial flash (T2) used for the ISP update.

The violet signal is the Chip select measured on the controller side (T1) used for the current measurement but not for the signal integrity checking.
VT2 (2.8V) – VT1 (2.4V) = 0.4V
R = 100Ohm
I = 0.4/100= 0.004A
The current injected in the controller is 4mA during the chip deselect.
The SPI signal from programmer to the serial flash (Yellow) is also reduced from 3.2V to 2.8V due to the Resistors protection of the programmer but still readable by the memory (CMOS input = Vcc/2) and ensure a good update.

Remark: The SPI communication between the application controller and the serial Flash is not concerned by these measurements.
For safe reason, the first trials must been started with SPI serial resistors value at 100 Ohm (controller protection for the first measurement) then if the current injected in the controller is safe enough, the serial resistors have to be reduced at lower value (47 Ohm, 33 Ohm) to ensure a good SPI signal during the application life (controller with Serial Flash). Actually, big resistor values will reduce the current injected in the controller during the ISP update but will filter the SPI signals during the communication between the controller and the serial flash. A small filtering is usually recommended on the SPI bus to reduce the overshoot and undershoot of the SPI

signals transitions. This will depend of the application frequency used and the parasitic capacitance of the board tracks (RC filter).

5.1.2 Application SPI control

User can also check if the controller can boot safely on the Serial Flash.

Step 1:
Supply the application to boot from the Serial Flash

Step 2:
The programmer can be kept connected on the ISP connector (transparent) if user does not start memory update from the DediProg software when the application is supplied.

Step 3:
The SPI signals quality can be checked with oscilloscope probes before and after the Serial resistors. DediProg recommends checking the SPI signals on the controller or Serial Flash **inputs side**:
- CS, Clock and MOSI on memory side (T2, T4 and T6)
- MISO on controller side (T7)

Remark 1: User can also notice the benefit of the Serial Resistors to filter the overshoot and undershoot of the SPI signals. Compare T1, T3, T5 and T8 (not filtered) with T2, T4, T6 and T7 (filtered).

Remark 2: User must take into consideration that the ISP Evaluation Board is a worst case for the application filtering. Actually, even if the Serial resistor value is reduced to 33 or 47 Ohm, the total parasitic capacitance of the ISP evaluation board is higher than the application parasitic capacitance so that the SPI filtering will be bigger (RC filter).

5.2 ISP update with application ON and resistors isolation

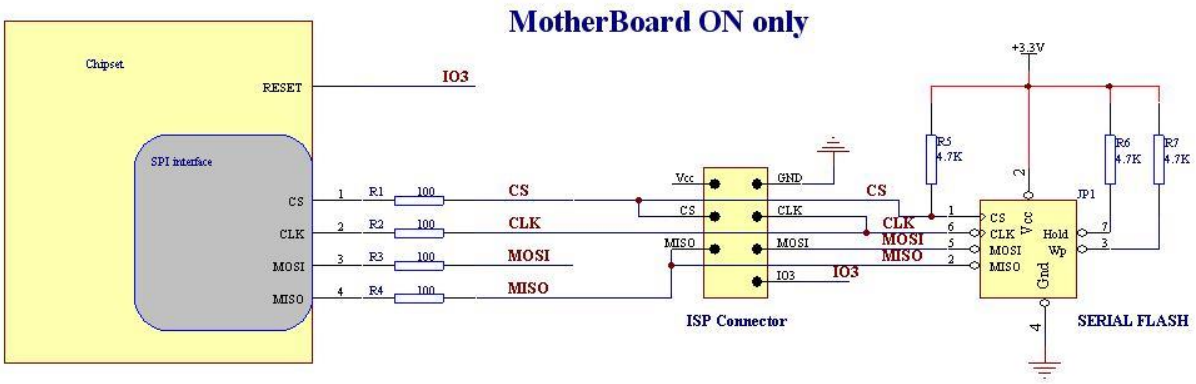
In this case, user must find an application condition during which the controller releases its SPI outputs in High Impedance so that the Serial Flash can be updated with application supplied and save the Vcc isolation (Diode or Mosfet).

Examples of application conditions with a probable High Impedance on SPI bus:
- Controller Reset
- Controller SPI in Stand-By (not used after boot)
- Dedicated mode for SPI High Impedance

User can check the controller SPI outputs in different application scenarios to find the High impedance. When the SPI High impedance is found, it can be used for Serial Flash ISP update.

Remark: Usually, the Controller Input MISO may always be in High Impedance when application is powered.

Fig 11: Equivalent schematic for Application



5.2.1 ISP Update control

Step 1:
Remove the supply from the application.

Step 2:
Solder 100 Ohm serial resistors on the ISP evaluation board SPI bus (R1, R2, R3, R4).
100 Ohm will protect the application controller and the programmer from conflict.
Others trials can be later performed with lower values (33 Ohm or 47 Ohm) when the SPI High Impedance conditions have been found.

Step3:
Vcc isolation is not needed in this case.
User must solder a 0 Ohm resistor on R7 (Short cut) and keep D1 and Q5 empty.

Step4:
Connect the ISP evaluation board to the application connector by using the dedicated cable provided with the kit.

Step5:
Connect the application power signals to the ISP evaluation board (keep the power off):

- Application Vcc to T10

Step6:
Connect the SF100 in the ISP connector of the ISP evaluation board.
Take care of the wrong connection (Fig3 and fig6)

Step7:
Supply the application.

Step8:
Enter the controller SPI High Impedance conditions (System Reset or any)
If the system must be switched in Reset mode, user can do it manually or uses our Programmer IO3 which is driven low automatically each time a Serial Flash update is started in the DediProg Software and driven high as soon as the update is finished. This can be achieved by connecting T12 or Con2 to the application System Reset signal. User will have to take care that this output is a Push Pull and not an open drain output.

Step9:
Connect the oscilloscope probes to measure the voltage on each SPI Serial resistors:
- On T1 and T2 to measure the threshold on R1 on Chip Select during the programmer communication with the Serial Flash.
- On T3 and T4 to measure the threshold on R2 on Clock during the programmer communication with the Serial Flash.
- On T5 and T6 to measure the threshold on R3 on MOSI during the programmer communication with the Serial Flash.
- On T7 and T8 to measure the threshold on R4 on MISO during the programmer communication with the Serial Flash.

Step10:
Launch the Serial flash update from the DediProg software to start the measurements.

Results Analysis:

- Communication for the Serial Flash update (between Programmer and Serial flash): SPI signals captured on T2, T4, T6 and T8 are used for the update. User must check their integrity taking care that the ISP evaluation board increase the capacitance (Worst case).

- Current measurement:
User has to measure the voltage through each SPI Serial resistors by calculating the difference of voltage between T1 and T2, T3 and T4, T5 and T6 then T7 and T8.
The Voltage through the Serial resistor will indicate if the controller SPI outputs are in High Impedance or not. The current calculated will highlight or not a conflict between the controller and the programmer: I = U/R.
For safe reason, the first trials must been started with SPI serial resistors value at 100 Ohm or higher (controller protection for the first measurement) then if no conflicts are detected, the serial resistors have to be reduced at lower value (47 Ohm, 33 Ohm) to ensure a good SPI signal during the application boot. A small filtering is usually recommended on the SPI bus to reduce the overshoot and undershoot of the SPI signals transitions. Big filtering will affect the integrity of the SPI signal between the controller and the serial flash (RC filter).

5.2.2 Application SPI control

User can also check if the controller can boot safely on the Serial Flash.

Step 1:
The programmer can be kept connected (transparent) if user does not start memory update when the application is supplied. If no update on going, the IO3 is driven High.

Step 2:
The SPI signals quality can be checked with oscilloscope probes before and after the Serial resistors. DediProg recommends checking the SPI signals on the controller or Serial Flash **inputs side**:

- CS, Clock and MOSI on memory side (T2, T4 and T6)
- MISO on controller side (T7)

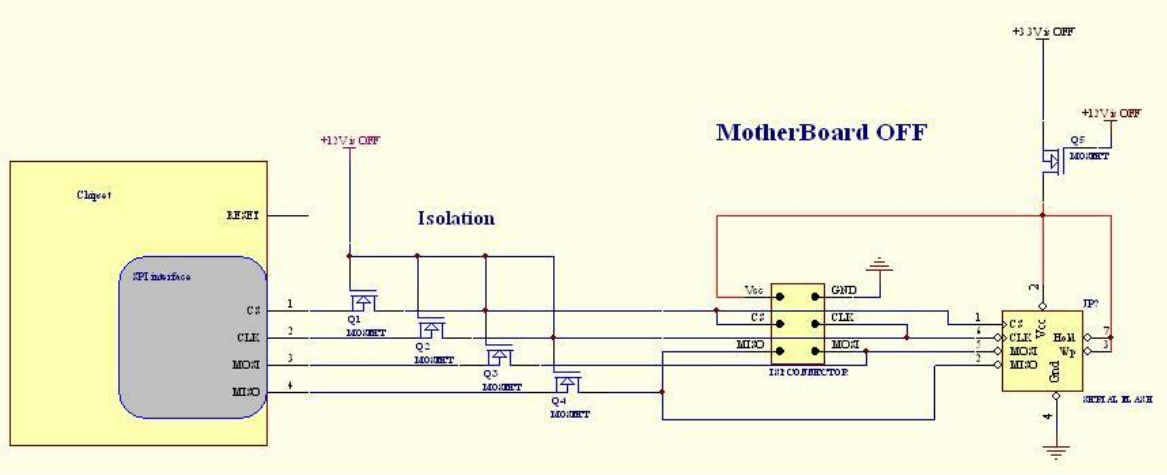
Remark 1: User can also notice the benefit of the Serial Resistor to filter the overshoot and undershoot of the SPI signals. Compare T1, T3, T5 and T8 (not filtered) with T2, T4, T6 and T7 (filtered).

Remark 2: User must take into consideration that the ISP Evaluation Board is a worst case for the application filtering. Actually, even if the Serial resistor value is reduced to 33 or 47 Ohm, the total parasitic capacitance of the ISP evaluation board is higher than the application parasitic capacitance so that the SPI filtering will be higher (RC filter). Application conditions will always be better.

5.3 ISP update with application OFF and MOSFET isolation

The application board, controller and the Serial Flash are not supplied by the application. In this case, the memory supply will be ensured by the Programmer during the duration of the update. MOSFET are used on SPI bus to isolate the controller from the programmer and Serial Flash during the ISP update.
This method works with any applications and controllers. MOSFET ensure a perfect isolation for the ISP update and perfect connection (small Ron) between controller and Serial Flash when application is running.

Fig 12: Equivalent schematic for Application



- The MOSFET are switched ON when the application is supplied and ensure a good communication between the controller and the serial Flash and a good supply of the Serial Flash with the application Vcc.
- The MOSFET are switched OFF when the application is not supplied and ensure a perfect isolation of the controller during the ISP update and of the programmer Vcc.

5.3.1 ISP Update control

Step 1:
Remove the supply from the application.

Step 2:
Solder the SPI "N MOSFET" on Q1, Q2, Q3, Q4

Step 3:
Select the Vcc isolation:
As the programmer will supply the Vcc to the memory during the update, the application must been isolated from it.

1) User can solder a Diode D1 so that the Vcc cannot be supplied from the programmer to the application but can still be supplied from the application to the Serial Flash when the Application is powered. The diode must been selected with a small threshold so that the application Vcc will still be in the serial Flash specification (2.7 to 3.6V).

2) User can also solder one N Mosfet Q5 for the Vcc isolation. The gate of the Mosfet is supplied by the application power (Vcc, 5V or 12V) so that when the application is not supplied, the MOSFET are switch OFF and prevent the programmer Vcc to supply the application board. When the application is supplied then the MOSFET is switched ON and the application Vcc can supply the memory.

One of this two methods must be selected and R7 must been kept empty.

Step 4:

Connect the ISP evaluation board to the application connector by using the dedicated cable provided with the kit.

Step 5:

Connect the application power signals to the ISP evaluation board (keep the power off):

- Application Vcc to T10
- Application Vcc or application 5V or 12V to Con1 to supply the MOSFET gates.

Step 6:

Connect the SF100 in the ISP connector of the ISP evaluation board.
Take care of the wrong connection (Fig3 and fig6)

Step 7:

Connect the oscilloscope probes to measure the voltage on each SPI MOSFET:
- On T2 to check the Chip Select signal during the programmer communication with the Serial Flash. No signal on T1 as Q1 is OFF.
- On T4 to check the Clock signal during the programmer communication with the Serial Flash. No signal on T3 as Q2 is OFF
- On T6 to check the MOSI signal during the programmer communication with the Serial Flash. No signal on T5 as Q3 is OFF
- On T8 to check the MISO signal during the programmer communication with the Serial Flash. No signal on T7 as Q4 is OFF

Step 8:

Launch the Serial flash update from the DediProg software with the application not powered to start the measurements.

Results Analysis:

- Communication for the Serial Flash update (between Programmer and Serial flash): SPI signals captured on T2, T4, T6 and T8 are used for the update. User must check their integrity.

- Isolation checking:

User will quickly notice by checking T1, T3, T5 and T7 that the MOSFET ensure a perfect isolation so that the controller is not impacted by the communication between the programmer and the Serial Flash.

5.3.2 Application SPI control

User can also check if the controller can boot safely on the Serial Flash.

Step 1:
The programmer can be kept connected (transparent) if user does not start memory update when the application is supplied.

Step 2:
Supply the application

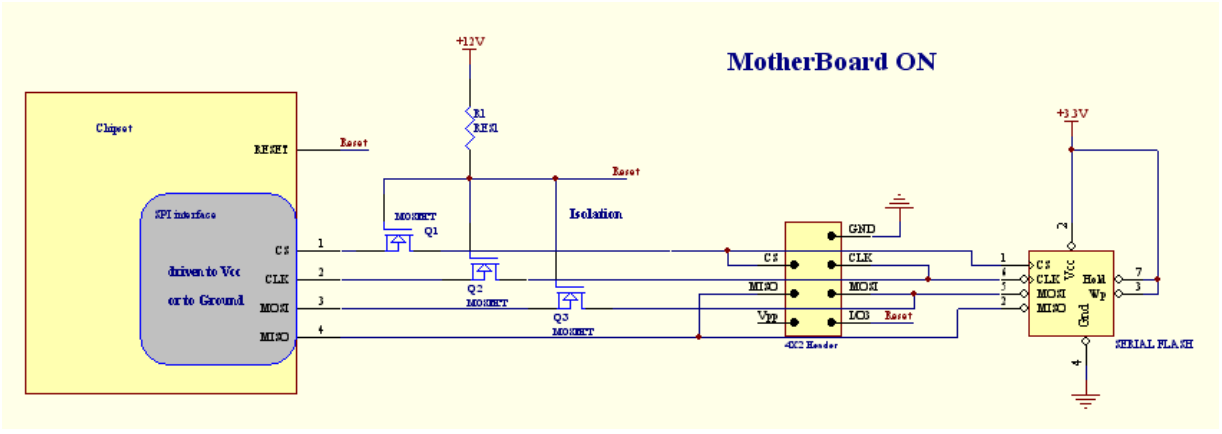
Step 3:
The SPI signals quality can be checked with oscilloscope probes on both sides of the the Mosfet:
- On T1 and T2 for Chip Select
- On T3 and T4 for Clock
- On T5 and T6 for MOSI
- On T7 and T8 for MISO

By comparing the signals on both sides of the Mosfet, User will notice that Mosfet ensure a good transfer of the signal.

5.4 ISP update with application ON and MOSFET isolation

In this case, the ISP update will be performed with the application supplied. 3 MOSFET are used on SPI bus to isolate the 3 controller outputs from the programmer and avoid a conflict. The Mosfet is not required on the MISO as it is a controller input (not conflict possible with the programmer) neither on the Vcc as the power is provided by the application.

Fig 13: Equivalent schematic for Application



- The MOSFET are switched ON when the application is supplied and ensure a good communication between the controller and the serial Flash.
- The MOSFET are switched OFF by the programmer IO3 which drives the Gate low each time a memory update is launched from the DediProg software and drive it high when the update is finished.

This method works with any applications and controllers and requires only 3 MOSFET. MOSFET ensure a perfect isolation for the ISP update and perfect connection (small Ron) between controller and Serial Flash when application is running.

5.4.1 ISP Update control

Step 1:
Remove the supply from the application.

Step 2:
- Solder the SPI "N MOSFET" on Q1, Q2 and Q3 (controller outputs) of the ISP Evaluation Board
- Solder a 33 or 47 Ohm resistor on R4 (controller input)

Step 3:
Vcc isolation is not needed in this case.
User must solder a 0 Ohm resistor on R7 (Short cut) and keep D1 and Q5 empty.

Step 4:
Connect the ISP evaluation board to the application connector by using the dedicated cable provided with the kit.

Step 5:
Connect the application power signals to the ISP evaluation board:
- Application Vcc to T10
- Application Vcc or application 5V or 12V to Con1 to supply the MOSFET gates.

Step 6:
Insert the strap on the Jump1 to connect the Programmer IO3 output to the Mosfet Gate. The IO3 will be driven low automatically each time an ISP update is started so that the MOSFET will be switched OFF during the operation completion. R8 ensures that there is no conflict between IO3 and application power (Con1).

Step 7:
Connect the SF100 in the ISP connector of the ISP evaluation board.
Take care of the wrong connection (Fig3 and fig6)

Step 8:
Connect the oscilloscope probes to measure the voltage on each SPI MOSFET or resistor:
- On T2 to check the Chip Select signal during the programmer communication with the Serial Flash. No signal on T1 as Q1 is OFF.
- On T4 to check the Clock signal during the programmer communication with the Serial Flash. No signal on T3 as Q2 is OFF
- On T6 to check the MOSI signal during the programmer communication with the Serial Flash. No signal on T5 as Q3 is OFF
- On T8 to check the MISO signal during the programmer communication with the Serial Flash.

Step 9:
Launch the Serial flash update from the DediProg software with the application not powered to start the measurements.

Results Analysis:

- Communication for the Serial Flash update (between Programmer and Serial flash): SPI signals captured on T2, T4, T6 and T8 are used for the update. User must check their integrity.

- Isolation checking:
User will quickly notice by checking T1, T3, T5 that the MOSFET ensure a perfect isolation so that the controller is not impacted by the communication between the programmer and the Serial Flash. The threshold measured on R4 between T8 and T7 will highlight if the master input MISO is in high impedance or not.

5.4.2 Application SPI control

User can also check if the controller can boot safely on the Serial Flash.

Step 1:
The programmer can be kept connected (transparent) if user does not start memory update when the application is supplied.

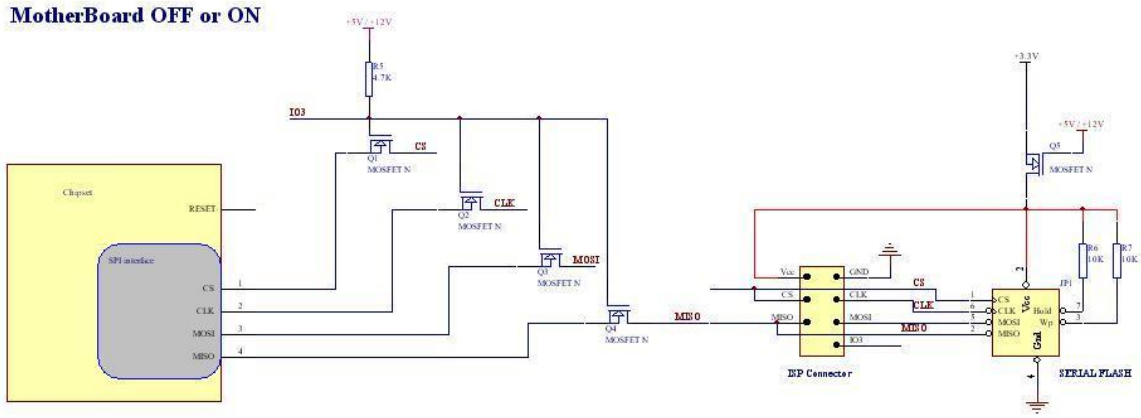
Step 2:
The SPI signals quality can be checked with oscilloscope probes on both sides of the the Mosfet or resistor during the application boot:
- On T1 and T2 for Chip Select (Mosfet)
- On T3 and T4 for Clock (Mosfet)
- On T5 and T6 for MOSI (Mosfet)
- On T7 and T8 for MISO (resistor)

By comparing the signals on both sides of the Mosfet, User will notice that Mosfet ensure a good transfer of the signal.

5.5 ISP update with application OFF or ON and MOSFET isolation

With this method the Serial Flash can be updated with application supplied or not.
5 Mosfet are used to isolate the controller SPI IO and the application Vcc during the update.

Fig 14: Equivalent schematic for Application



- The MOSFET are switched ON when the application is supplied and ensure a good communication between the controller and the serial Flash and a good supply of the Serial Flash with the application Vcc.
- The MOSFET are switched OFF automatically when the application is not supplied or by the programmer IO3 when the update is started with application supplied.

This method works with any applications and controllers. MOSFET ensure a perfect isolation for the ISP update and perfect connection (small Ron) between controller and Serial Flash when application is running.

5.5.1 ISP Update control

Step 1:
Remove the supply from the application.

Step 2:
Solder the SPI "N MOSFET" on Q1, Q2, Q3, Q4

Step 3:
Select the Vcc isolation:
As the programmer will supply the Vcc to the memory during the update, the application must been isolated from it.

1) User can solder a Diode D1 so that the Vcc cannot be supplied from the programmer to the application but can still be supplied from the application to the Serial Flash when the Application is powered. The diode must been selected with a small threshold so that the application Vcc will still be in the serial Flash specification (2.7 to 3.6V).

2) User can also solder one N Mosfet Q5 for the Vcc isolation. The gate of the Mosfet is supplied by the application power (Vcc, 5V or 12V) so that when the application is not supplied, the MOSFET are switch OFF and prevent the programmer Vcc to supply the

application board. When the application is supplied then the MOSFET is switched ON and the application Vcc can supply the memory.

One of this two methods must be selected and R7 must been kept empty.

Step 4:

Connect the ISP evaluation board to the application connector by using the dedicated cable provided with the kit.

Step 5:

Connect the application power signals to the ISP evaluation board (keep the power off):

- Application Vcc to T10
- Application Vcc or application 5V or 12V to Con1 to supply the MOSFET gates.

Step 6:

Insert the strap on the Jump1 to connect the Programmer IO3 output to the Mosfet Gate. The IO3 will be driven low automatically each time an ISP update is started so that the MOSFET will be switched OFF during the operation completion. R8 ensures that there is no conflict between IO3 and application power (Con1).

Step 7:

Connect the SF100 in the ISP connector of the ISP evaluation board.
Take care of the wrong connection (Fig3 and fig6)

Step 8:

Connect the oscilloscope probes to measure the voltage on each SPI MOSFET:

- On T2 to check the Chip Select signal during the programmer communication with the Serial Flash. No signal on T1 as Q1 is OFF.
- On T4 to check the Clock signal during the programmer communication with the Serial Flash. No signal on T3 as Q2 is OFF
- On T6 to check the MOSI signal during the programmer communication with the Serial Flash. No signal on T5 as Q3 is OFF
- On T8 to check the MISO signal during the programmer communication with the Serial Flash. No signal on T7 as Q4 is OFF

Step 9:

Launch the Serial flash update from the DediProg software with the application supplied and with the application not supplied to start the measurements.

Results Analysis:

- Communication for the Serial Flash update (between Programmer and Serial flash): SPI signals captured on T2, T4, T6 and T8 are used for the update. User must check their integrity.

- Isolation checking:

User will quickly notice by checking T1, T3, T5 and T7 that the MOSFET ensure a perfect isolation so that the controller is not impacted by the communication between the programmer and the Serial Flash.

5.5.2 Application SPI control

User can also check if the controller can boot safely on the Serial Flash.

Step 1:
The programmer can be kept connected (transparent) if user does not start memory update when the application is supplied.

Step 2:
The SPI signals quality can be checked with oscilloscope probes on both sides of the the Mosfet during the application boot:
- On T1 and T2 for Chip Select
- On T3 and T4 for Clock
- On T5 and T6 for MOSI
- On T7 and T8 for MISO

By comparing the signals on both sides of the Mosfet, User will notice that Mosfet ensure a good transfer of the signal.

VI. ISP Evaluation Kit content

User will find in the kit, all the equipment needed for the ISP evaluation in the different possible conditions.

ISP Evaluation Kit content:

- **1 SF100 programmer** to update the serial Flash on board with ISP and USB cables included
- **1 ISP Evaluation board:** To test and validate the ISP method with your controller on your application.
- **1 Flat cable:** to connect the ISP evaluation board to the application
- **2 SMT 1.27mm connectors:** to solder in place of your application Serial Flash
- **10 resistors:** 100 Ohm for safe SPI isolation trials
- **10 resistors:** 47 Ohm for tuned SPI isolation trials
- **2 resistors:** 0 Ohm for Vcc short cut
- **10 N MOSFET** for SPI and Vcc isolation trials
- **2 Diodes:** for Vcc isolation trials
- **1 Strap:** to connect programmer IO3 to MOSFET gates
- **3 cables with test clip:** to connect the application Vcc, High voltage (for Mosfet driving) and reset to the ISP evaluation board

VII. Revision History

Date	Version	Changes
2009/12/02	V1.0	Initial release.
2017/07/27	V1.1	Adjusted document formats and changed company address.

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